

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/749,977	12/30/2003	Robert G. Wodnicki	. RD-29,494	9676	
41838 GENERALEI	7590 05/03/200 FCTRIC COMPANY	•	EXAMINER		
GENERAL ELECTRIC COMPANY (PCPI) C/O FLETCHER YODER			JAWORSKI, FRANCIS J		
P. O. BOX 692289 HOUSTON, TX 77269-2289			ART UNIT	PAPER NUMBER	
,			3768		
			MAIL DATE	DELIVERY MODE	
	•		05/03/2007	PAPER	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

			೮
	Application No.	Applicant(s)	
055 4-41	10/749,977	WODNICKI ET AL.	
Office Action Summary	Examiner	Art Unit	
	Jaworski Francis J.	3768	
The MAILING DATE of this communication a Period for Reply	ppears on the cover sheet wi	th the correspondence address	
A SHORTENED STATUTORY PERIOD FOR REP WHICHEVER IS LONGER, FROM THE MAILING  - Extensions of time may be available under the provisions of 37 CFR 1 after SIX (6) MONTHS from the mailing date of this communication.  - If NO period for reply is specified above, the maximum statutory perior Failure to reply within the set or extended period for reply will, by state Any reply received by the Office later than three months after the mail earned patent term adjustment. See 37 CFR 1.704(b).	DATE OF THIS COMMUNIC  1.136(a). In no event, however, may a red  d will apply and will expire SIX (6) MON  tte. cause the application to become AB	CATION.  apply be timely filed  THS from the mailing date of this communication.  ANDONED (35 U.S.C. & 133)	
Status			
1) Responsive to communication(s) filed on 12-	30-03 IDS.		
	is action is non-final.	:	
3) Since this application is in condition for allow	ance except for formal matte	ers, prosecution as to the merits is	
closed in accordance with the practice under	Ex parte Quayle, 1935 C.D	. 11, 453 O.G. 213.	
Disposition of Claims	•		
4) ⊠ Claim(s) 1 - 25 is/are pending in the application 4a) Of the above claim(s) is/are withdrest 5) ⊠ Claim(s) 22 - 25 is/are allowed.  6) ⊠ Claim(s) 1,7,9,13 and 18-21 is/are rejected.  7) ⊠ Claim(s) 2-6,8,10-12 and 14-17 is/are objected.  8) □ Claim(s) are subject to restriction and	awn from consideration.		
Application Papers			
9)☐ The specification is objected to by the Examir	ner		
10)⊠ The drawing(s) filed on <u>30 December 2003</u> is		objected to by the Examiner.	
Applicant may not request that any objection to the			
Replacement drawing sheet(s) including the corre			
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:  1. Certified copies of the priority document copies of the priority document copies of the certified copies of the priority document copies of the certified copies of the priority document copies of the certified copies of the priority document copies of the certified copies of the priority document copies of the certified copies of the priority document copies of the certified copies of the priority document copies.	nts have been received. nts have been received in A ority documents have been au (PCT Rule 17.2(a)).	oplication No received in this National Stage	
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO/SB/08)	Paper No(s	ummary (PTO-413) )/Mail Date formal Patent Application	
Paper No(s)/Mail Date <u>12-30-03</u> .	6)  Other:	* *	

## **DETAILED ACTION**

## **Drawings**

Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated, according to the specification page 6 lines 13 - 17. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

## Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation

Art Unit: 3768

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 7, 9, 13, 18 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Savord et al (US6380766) alone or further in view of Smith et al (US5744898), alone or further in view of Leavitt et al (US6540682) or Miller et al (US5740846).

Savord et al teaches an integrated circuit 10 in association with an ultrasonic imaging array of individual transducer elements 20, where the integrated circuit 10 comprises a high voltage pulser 14, 24 a receive section amplifier 18 and transmit /receive switch 15 operative during the control of operational phasing, where the receive amplifier is protected in a first transmit state of the switch and unprotected during a second receive phase of the switch, but does not use a switch designated per se 'low voltage' for element 16, see col. 9 lines 30 – 55. However it is argued that Savord would include at least some low voltage control of this switch since power consumption is an IC constraint, and therefore the switch would be low voltage in terms of control under this argument.

A common drain configuration for the high voltage pulser is shown for example in fig. 11.

In the alternative, Smith et al teaches that when the transducer array for a handheld ultrasound probe or 2D such probe is made more efficient such as by multi-layering, then the transmit circuitry overall may be made lower voltage, see col. 16 lines 49 – 52.

In supplement thereto, Leavitt et al, cols. 4 – 5 bridging teaches that an ASIC architecture may be used to incorporate the front-end electronics into a probe, whereupon the lower voltage overall would result from such an integrated circuit having economy-of-scale.

In alternative supplement, Miller et al taught that when low voltage transmit/receive switching is applied to array transducers, slow response and switchover glitches are avoided, see col. 2 lines 25 – 38 and col. 7 discussion of Fig. 6, and therefore it would have been desirable to incorporate such into Savord alone or as modified for transducer efficiency per Smith et al.

## Allowable Subject Matter

Claims 2 –6, 8, 10 – 12, 14 - 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 22 – 25 are allowed.

Art Unit: 3768

Patentability Assessment

Patentability for the base claims is currently being opposed under the arguments that a) Savord taught use of a CMOS/low voltage transmit and receive circuit where the transmit/receive isolation switch would include at least some low voltage portions such as its control input, and in supplement thereto b) Smith et al taught that where the transducer is made as a laminate then 'lower' voltages may be used through-out, in which case the claimed 'low' voltage encounters a 'relative to what' argument, or (c) that the modernizing tendency in the art is was fabricate the front end electronics in ASIC architecture anyway (Leavitt et al), or (d) that the switching of transducer groupings was known to have been improved by low voltage application in a variety of forms since higher speed and less glitching artifact occurred (Miller).

Any inquiry concerning this communication should be directed to Jaworski Francis J. at telephone number 571-272-4738.

FJJ:fjj

4-24-07

Francis J. Jaworski Primary Examiner